**Pipelined Processor IF stage Lab**

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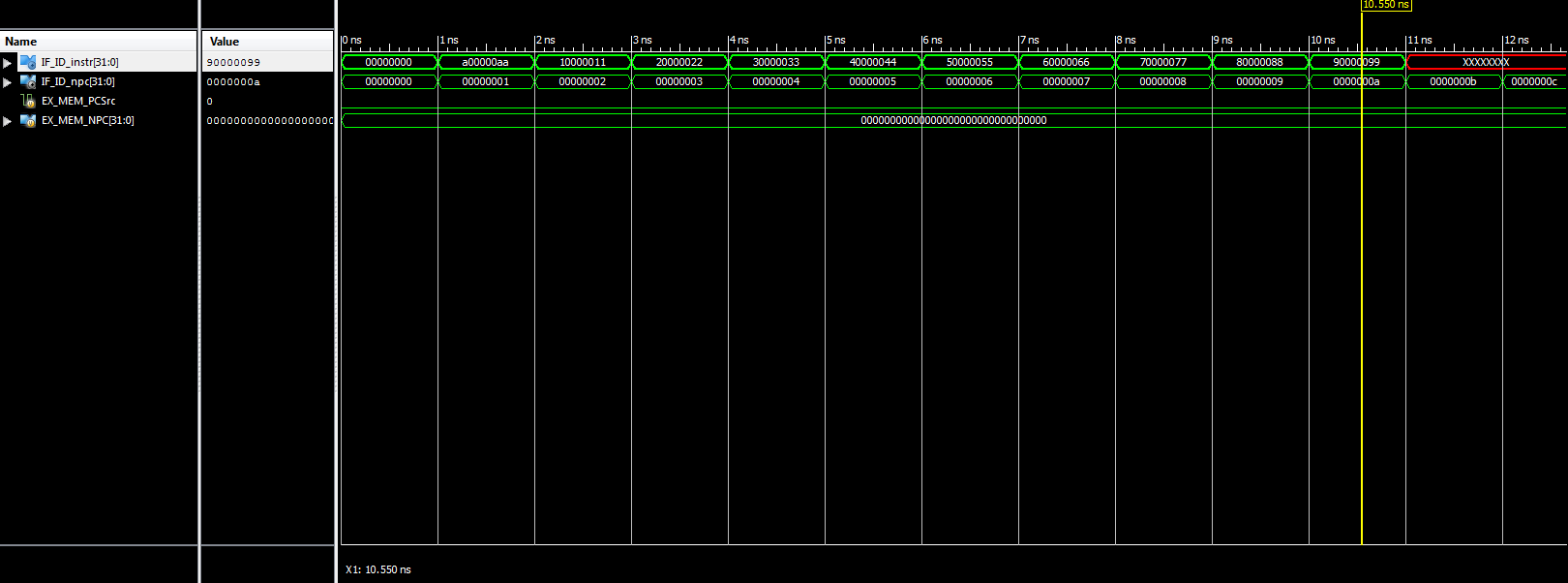
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**12 January 2021**

**CSE 4010 Winter 2021**

The Instruction Fetch stage fetches the next instruction from memory using the address in the Program Counter register, which contains the address for the next instruction and stores this instruction in the Instruction Register. The instruction memory will then respond by sending the correct instruction. Lab one consists of implementing the IF (Instruction Fetch) stage and testing the fetching of instructions from the memory of every cycle.

The EX\_MEM\_PCSrc is a pipeline buffer register. The EX\_MEM\_N PC is the buffers’ pc and at the moment of initialization the first 10 addresses with what’s in the memory module. The simulation of the test bench gives the following:



With a text output of:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Time** | **PC** | **NPC** | **Dataout of MEM** | **IF\_ID\_instr** | **IF\_ID\_NPC** |
| 0 | 0 | 1 | a00000aa | 00000000 | 0 |
| 1 | 1 | 2 | 10000011 | a00000aa | 1 |
| 2 | 2 | 3 | 20000022 | 10000011 | 2 |
| 3 | 3 | 4 | 30000033 | 20000022 | 3 |
| 4 | 4 | 5 | 40000044 | 30000033 | 4 |
| 5 | 5 | 6 | 50000055 | 40000044 | 5 |
| 6 | 6 | 7 | 60000066 | 50000055 | 6 |
| 7 | 7 | 8 | 70000077 | 60000066 | 7 |
| 8 | 8 | 9 | 80000088 | 70000077 | 8 |
| 9 | 9 | 10 | 90000099 | 80000088 | 9 |
| 10 | 10 | 11 | xxxxxxxx | 90000099 | 10 |

When the test runs past PC 10, the Dataout of MEM is undefined, and outputs end up as xxxxxxxx.